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EXAMINER	
VELEZ, ROBERTO	

ART UNIT	PAPER NUMBER
2829	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

EFIPLAW@US.IBM.COM

Office Action Summary	Application No.	Applicant(s)	
	10/595,526	PASTEL, LEAH M. P.	
	Examiner	**Art Unit**	
	Roberto Velez	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _02 December 2008_.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-25_ is/are pending in the application.

4a) Of the above claim(s) _1-8 and 25_ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _9-24_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 12/02/2008 have been fully considered but they are not persuasive.

Regarding claim 9, Applicant argues that Jennion does not teach nor suggest a separate quiescent power distribution. The Examiner respectfully disagrees. Jennion discloses V1 powering the DUT, which is a high power supply and V4 power de DUT, which is a low current power supply used for measuring high resolution static current consumption (quiescent current of the DUT (Col. 3, Ln 25-39). Therefor, Jennion does teach nor suggest a separate quiescent power distribution (V4).

In addition, Applicant argues that Teene does not teach separate global and quiescent power supply busses within the chip. The Examiner respectfully disagrees. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., separate) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Even though, Teene shows wherein the Vss supply 16 and the Vss internal supply 14 electrically connected, they are still considered separate elements with different functions.

Regarding claim 10, Applicant argues that Applicant's teaching of hot switching is purposely required to effectively make IDDQ measurements for different voltage island combinations without having to reapply the conditioning test pattern. The combination of

Jennion to Teene is unable to achieve this. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., hot switching is purposely required to effectively make IDDQ measurements for different voltage island combinations without having to reapply the conditioning test pattern) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Regarding claim 11, Applicant argues that the present application teaches two separate voltage connections (power planes) and voltage distribution networks within the chip, which may be connected to two independent voltages supplied by two different power supplies. The combination of Jennion and Teene does not. The Examiner respectfully disagrees. Jennion et al. discloses supplying a voltage VDDg [V1, V2 or V3] to the global voltage bus [117, 119 or 121]; and supplying a voltage VDDq [V4] to the quiescent voltage bus [123] (Col. 3, Ln 1-41).

Regarding claims 13-14, Applicant argues that neither Jennion nor Teene teaches a header device as shown in Applicant's Fig. 1. Applicant shows in fig. 1 wherein a header device is a device that connects voltage islands (sinks) to the power distribution. The Examiner respectfully disagrees. Claims 13 and 14 recite "providing a **connection** between the voltage island and the global and quiescent voltage busses, wherein the **connection** includes a header device". Jennion shows (fig. 1) "providing a **connection** [116, 118, 120 or 122] between each voltage island [104] and the global

and quiescent voltage busses [117, 119, 121 or 123], wherein each **connection** [116, 118, 120 or 122] includes a header device [116, 118, 120 or 122]". Therefor, claims 13-14 does not particularly distinguish the header device recited from the header device disclosed in Jennion.

Regarding claims 12 and 22, Applicant argues that Akiki teaches away from Applicant's teaching. The Examiner respectfully disagrees. Akiki was merely used to demonstrate that is well known to have VDDg equal to VDDq. This does not make the combination of Jennion, Teene and Akiki inoperable, since the apparatus of Jennion will still operate by applying the same voltage to the voltage buses.

Regarding claim 16, Applicant argues that extending Jennion-Teene with Sugasawaea for multiple sections requires additional power supplies and selectable power supply lines. The Examiner respectfully disagrees. Even though, extending Jennion-Teene with Sugasawaea for multiple sections requires additional power supplies and selectable power supply lines, nevertheless, it discloses the claimed limitations.

Regarding claim 17, Applicant argues that Cole is being interpreted incorrectly by the Office Action. The Examiner respectfully disagrees. Cole, Jr. et al. discloses locating IDDQ defects using a resistance of a resistive load (Col. 7, Ln 44-55). Even though, Cole, Jr. et al. does not specifically disclose a resistance of the quiescent voltage bus, it does teach using the resistance of a device to locate an IDDQ defect.

Regarding claim 18, Applicant argues that Applicant teaches IDDQ testing on individual voltage islands or groups of voltage islands for additional purposes besides

locating defects within the chip. In response to applicant's argument that Applicant teaches IDDQ testing on individual voltage islands or groups of voltage islands for additional purposes besides locating defects within the chip, the fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985).

Regarding claim 20, Applicant argues that it cannot find any reference in Inoshita to IDDQ measurements for similar circuitry, and thus, Applicant cannot place Inoshita teaching in its context. In response, the Examiner contents that claim 20 is recited in alternatively form (or). The prior art is required to disclose either one of the two limitations recited. The Examiner addressed the second limitation which was “wherein the obtained IDDQ measurements are compared to an average IDDQ measurement”.

Regarding claim 23, Applicant argues that Inoshita does not disclose a method of localizing an IDDQ defect within the chip. In response to applicant's argument that the references fail to show certain features of applicant’s invention, it is noted that the features upon which applicant relies (i.e., localizing an IDDQ defect within the **chip**) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Claim Objections

2. Claims 9-25 are objected to because of the following informalities:

Claims 9 and 21 recite the term “V-islands”. To keep consistency in the claim language with respect to the language used in the specification, Applicant is encouraged to recite “Voltage islands”.

Claim 25 was previously withdrawn in the election filed on 07/08/2008 and now is labeled “currently amended”. The correct labeling for claim 25 is “withdrawn”. Appropriate correction is required.

Claims 10-20 and 22-24 depending from claims 9 or 21 are objected for the same reasons.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 9-11, 13-16, 18, 21 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jennion et al. (US Pat. 5,721,495) in views of Sugasawara (US Pat. 6,043,672) and Teene (US Pat. 5,726,997).

Regarding claim 9, Jennion et al. shows (Figures 1-6) a method of performing a quiescent current (IDDQ) test of a chip having voltage island coupled to control logic, the method comprising: powering the chip [102] through at least one global voltage line (either one of 117, 119 or 121) and setting (using 106 and 130) the chip in a quiescent

state; hot-switching (using 124) at least one of the voltage islands [104] between a global voltage line (either one of 117, 119 or 121) and a quiescent voltage line [123]; and measuring (using 130 and 106) the IDDQ on the at least one voltage island [104] (as shown in fig. 6).

Jennion et al. fails to disclose performing an IDDQ test of a chip having voltage islands and wherein the global voltage line and the quiescent voltage line are buses. However, Sugasawara shows (Fig. 1) performing an IDDQ test of a chip [10] having voltage islands [12, 14, 16] and Teene shows (Figures 1-2) a global voltage bus [16] and a quiescent voltage bus [14].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Sugasawara and Teene into the device of Jennion et al. by performing an IDDQ test of a chip having voltage islands and using a global voltage bus and a quiescent voltage bus instead of a global voltage line and a quiescent voltage line. The ordinary artisan would have been motivated to modify Jennion et al. in the manner set forth above for the purpose of being able to simultaneously or alternatively receive and apply different voltage values to a chip having voltage islands and verify the operation of the voltage islands.

Regarding claim 10, the combination of Jennion et al., Sugasawara and Teene discloses everything as claimed above in claim 9; in addition, Jennion et al. discloses wherein each of the at least one voltage islands does not lose state during the hot-switching between the quiescent and global voltage busses (Col. 3, Ln 25-39 and

specifically Col. 6, Ln 37-39 discloses simultaneously deselecting a power supply and selecting a second power supply in a quiescent state).

Regarding claim 11, the combination of Jennion et al., Sugasawara and Teene discloses everything as claimed above in claim 9; in addition, Jennion et al. discloses supplying a voltage VDDg [V1, V2 or V3] to the global voltage bus [117, 119 or 121]; and supplying a voltage VDDq [V4] to the quiescent voltage bus [123] (Col. 3, Ln 1-41).

Regarding claim 13, the combination of Jennion et al., Sugasawara and Teene discloses everything as claimed above in claim 9; in addition, Jennion et al. shows (Fig. 1) wherein hot-switching further comprises: providing a connection [116, 118, 120 or 122] between each of the at least one voltage islands and the global and quiescent voltage busses [117, 119, 121 or 123]; and selecting (using 124) at least one of the connections [116, 118, 120 or 122] to connect each of the at least one voltage islands to at least one of the global and quiescent voltage busses [117, 119, 121 or 123].

Regarding claim 14, the combination of Jennion et al., Sugasawara and Teene discloses everything as claimed above in claim 13; in addition, Jennion et al. shows (Fig. 1) wherein each connection [116, 118, 120 or 122] includes a header device [116, 118, 120 or 122], and wherein each connection [116, 118, 120 or 122] is selected (using 124) by activating the header device of the connection via a control signal [124] (Col. 3, Ln 1-65).

Regarding claim 15, the combination of Jennion et al., Sugasawara and Teene discloses everything as claimed above in claim 9; in addition, Jennion et al. discloses wherein performing IDDQ testing comprises: applying a test pattern (voltage from the

power supplies) to each of the at least one voltage islands, wherein the test pattern remains valid during hot-switching between the global and quiescent voltage busses (Col. 3, Ln 25-39 and specifically Col. 6, Ln 37-39 discloses simultaneously deselecting a power supply and selecting a second power supply in a quiescent state).

Regarding claim 16, the combination of Jennion et al., Sugasawara and Teene discloses everything as claimed above in claim 9.

The combination of Jennion et al. and Teene fails to disclose hot-switching different sets of voltage islands between the global and quiescent voltage busses. However, Sugasawara discloses hot-switching (using 24 or 25) different sets of voltage islands [12, 14 or 16] between the global [30] and quiescent voltage busses [26 or 28] (Col. 4, Ln 10-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Sugasawara into the device of the combination of Jennion et al. and Teene by hot-switching different sets of voltage islands between the global and quiescent voltage busses. The ordinary artisan would have been motivated to modify the combination of Jennion et al. and Teene in the manner set forth above for the purpose of testing a plurality of voltage islands either simultaneously or alternatively.

Regarding claim 18, the combination of Jennion et al., Sugasawara and Teene discloses everything as claimed above in claim 9.

The combination of Jennion et al. and Teene fails to disclose wherein IDDQ testing is performed on individual voltage islands or sets of voltage islands. However,

Sugasawara shows (Figures 2-3) wherein IDDQ testing is performed on individual voltage islands or sets of voltage islands (Col. 5, Ln 27 through Col. 6, Ln 55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Sugasawara into the device of the combination of Jennion et al. and Teene by performing IDDQ testing on individual voltage islands or sets of voltage islands. The ordinary artisan would have been motivated to modify the combination of Jennion et al. and Teene in the manner set forth above for the purpose of identifying areas of unusual quiescent current consumption.

Regarding claim 21, Jennion et al. shows (Figures 1-6) a method, comprising: powering (using 108 and 130) a chip [102, 104] having voltage island coupled to control logic [106, 130] at least one global voltage line (either one of 117, 119 or 121) and setting (using 106 and 130) the chip in a quiescent state; hot-switching (using 124) at least one voltage islands [104] between a plurality of different voltage lines (either one of 117, 119, 121 or 123) wherein each voltage island [104] does not lose state during the hot-switching (Col. 3, Ln 25-39 and specifically Col. 6, Ln 37-39 discloses simultaneously deselecting a power supply and selecting a second power supply in a quiescent state); and measuring (using 130 and 106) a quiescent current (IDDQ) on the at least one voltage island (as shown in fig. 6).

Jennion et al. fails to disclose a chip having voltage islands and wherein the global voltage line and the quiescent voltage line are buses. However, Sugasawara shows (Fig. 1) performing an IDDQ test of a chip [10] having voltage islands [12, 14, 16]

and Teene shows (Figures 1-2) a global voltage bus [16] and a quiescent voltage bus [14].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Sugasawara and Teene into the device of Jennion et al. by performing an IDDQ test of a chip having voltage islands and using a global voltage bus and a quiescent voltage bus instead of a global voltage line and a quiescent voltage line. The ordinary artisan would have been motivated to modify Jennion et al. in the manner set forth above for the purpose of being able to simultaneously or alternatively receive and apply different voltage values to a chip having voltage islands and verify the operation of the voltage islands..

Regarding claim 24, the combination of Jennion et al., Sugasawara and Teene discloses everything as claimed above in claim 21; in addition, Jennion et al. discloses wherein the voltage busses (either one of 117, 119, 121 or 123) comprise power supply busses or ground busses (Col. 3, Ln 25-39).

5. Claims 12 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jennion et al. (US Pat. 5,721,495), Sugasawara (US Pat. 6,043,672) and Teene (US Pat. 5,726,997) as applied to claims 11 and 21 above, and further in view Akiki et al. (US Pat. 5,294,883).

Regarding claim 9, the combination of Jennion et al., Sugasawara and Teene discloses everything as claimed above in claim 11.

The combination of Jennion et al., Sugasawara and Teene fails to disclose wherein VDDg is equal to VDDq. However, Akiki et al. shows (Fig. 3) wherein VDDg is equal to VDDq (at step 32 and 34 disclose wherein VTT (VDDq) is equal to VDD).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Akiki et al. into the device of the combination of Jennion et al., Sugasawara and Teene by using same voltages for VDDg and VDDq. The ordinary artisan would have been motivated to modify the combination of Jennion et al., Sugasawara and Teene in the manner set forth above for the purpose of using a single power supply to save cost.

Regarding claim 22, the arguments used for the rejection of claims 11-12 and 21 regarding this feature, also apply.

6. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jennion et al. (US Pat. 5,721,495), Sugasawara (US Pat. 6,043,672) and Teene (US Pat. 5,726,997) as applied to claim 9 above, and further in view Cole, Jr. et al. (US Pat. 6,031,386).

Regarding claim 17, the combination of Jennion et al., Sugasawara and Teene discloses everything as claimed above in claim 9.

The combination of Jennion et al., Sugasawara and Teene fails to disclose locating IDDQ defects using a resistance of the quiescent voltage bus. However, Cole, Jr. et al. discloses locating IDDQ defects using a resistance of a resistive load (Col. 7, Ln 44-55). Even though Cole, Jr. et al. does not specifically disclose a resistance of the

quiescent voltage bus, it does teach using the resistance of a device to locate an IDDQ defect.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Cole, Jr. et al. into the device of the combination of Jennion et al., Sugasawara and Teene by locating IDDQ defects using a resistance of the quiescent voltage bus. The ordinary artisan would have been motivated to modify the combination of Jennion et al., Sugasawara and Teene in the manner set forth above for the purpose of accurately monitoring the operation of the voltage island.

7. Claims 19-20 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jennion et al. (US Pat. 5,721,495), Sugasawara (US Pat. 6,043,672) and Teene (US Pat. 5,726,997) as applied to claims 9 and 21 above, and further in view of Inoshita et al. (US PGPUB 2002/0186035).

Regarding claim 19, the combination of Jennion et al., Sugasawara and Teene discloses everything as claimed above in claim 9.

The combination of Jennion et al. and Teene fails to disclose obtaining IDDQ measurements from individual voltage islands or sets of voltage islands during the IDDQ testing; and comparing the obtained IDDQ measurements to other IDDQ measurements. However, Sugasawara shows (Figures 2-3) obtaining IDDQ measurements from individual voltage islands [12, 14 or 16] or sets of voltage islands during the IDDQ testing (Col. 5, Ln 27 through Col. 6, Ln 55) and Inoshita et al.

discloses comparing the obtained IDDQ measurements to other IDDQ measurements (Page 2, Paragraphs 0011 and 0012).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Sugasawara and Inoshita et al. into the device of the combination of Jennion et al. and Teene by locating IDDQ defects using a resistance of the quiescent voltage bus and comparing the obtained IDDQ measurements to other IDDQ measurements. The ordinary artisan would have been motivated to modify the combination of Jennion et al. and Teene in the manner set forth above for the purpose of monitoring the operation of the voltage islands and accurately monitoring the operation of the voltage islands.

8. Regarding claim 20, the combination of Jennion et al., Teene, Sugasawara and Inoshita et al. discloses everything as claimed above in claim 19; in addition, Inoshita et al. discloses wherein the obtained IDDQ measurements are compared to IDDQ measurements for similar circuitry, or wherein the obtained IDDQ measurements are compared to an average IDDQ measurement (Page 2, Paragraphs 0011 and 0012).

Regarding claim 23, the combination of Jennion et al., Sugasawara and Teene discloses everything as claimed above in claim 21.

The combination of Jennion et al., Sugasawara and Teene fails to disclose locating IDDQ defects in the at least one voltage island. However, Inoshita et al. discloses locating IDDQ defects in the at least one voltage island [1] (Page 2, Paragraphs 0011 and 0012).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Inoshita et al. into the device of the combination of Jennion et al., Sugasawara and Teene by locating IDDQ defects in the at least one voltage island. The ordinary artisan would have been motivated to modify the combination of Jennion et al., Sugasawara and Teene in the manner set forth above for the purpose of monitoring the voltage island to verify that proper operation is being done.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

10. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Roberto Velez whose telephone number is 571-272-8597. The examiner can normally be reached on Monday-Friday 8:00am- 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on 571-272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Roberto Velez/
Examiner, Art Unit 2829
03/11/2009

/Ha T. Nguyen/
Supervisory Patent Examiner, Art Unit 2829